## sdmay18-13: Measuring Voltage and Wire Continuity

Week 10 Report
November 12 - November 18

## Team Members

Aaron Eaton — *Chief Engineer*
Mohamed Almansoori — *Report Manager*
Christopher Williams — *Test Engineer*
Samuel Kline — *Meeting Facilitator*
Matthew Kelly — *Meeting Scribe*

## Summary of Progress this Report

Voltage: Tested capacitor divider and op amp circuits.

Wire Continuity: improved block diagram with values that we can use as a better example of our solution

## Pending Issues

Voltage: Unexpected results from simulating capacitor divider circuit.

Unexpected results from simulating op amp circuit, need to simplify the circuit.
Wire Continuity: still don't know if it works

## Plans for Upcoming Reporting Period

Voltage: Compile results of different approaches that we have tested and prepare them for the semester's final presentation.

Wire Continuity: need to test it

## Individual Contributions

| Team Member | Contribution | Weekly Hours | Total Hours |
|---|---|---|---|
| Aaron Eaton | Learned more about couplers, found out db loss is a certain percentage of the signal that gets lost in coupling, for example a 20db coupler loses about 90% of the signal. Made a better block diagram showing exact values for the signal being sent and the coupling db as well as the parts we can use to send the signal and the coupler. | 4 | 54 |
| Mohamed Almansoori | In this last week, we were wrapping everything that we needed to do the presentation next week as well as for design document. I will give a presentation about all | 5 | 51 |

| | | | |
|---|---|---|---|
| | the different wire continuity diagnosis methods I researched and how it does work in our project. While Aaron came up with a promising solution using a directional coupler, we can continue working on that next semester so later on we can prototype it. | | |
| Christopher Williams | Worked on simulating phase to neutral AC/DC voltage measuring circuit in multisim. Circuit worked with some non ideal op amp behavior, including voltage being clipped sooner than expected. Circuit was more complex than necessary, and will be simplified once non ideal behavior has been worked out. | 6 | 59 |
| Samuel Kline | Finalizing documentation for the voltage portion of our project. Design document and Project Plan needed to be updated and progress reports for previous weeks needed to be completed. Started work on material for final presentation. | 4 | 47.5 |
| Matthew Kelly | Worked on trying to get the capacitor divider circuit simulation, using MultiSim, to match what was expected of it. However, I could not really find out why the full wave rectified voltage waveform would reach a negative voltage or why there was so much noise in what would be the negative part of the AC waveform. Also, the ratios were not giving the expected results of being between 1.5V and 5V. | 6 | 52 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |